DC-50GHz MMIC Variable Attenuator with a 30dB Dynamic Range

Hiroshi Kondoh

Hewlett-Packard Co.
Microwave Technology Division
Santa Rosa, CA 95401

Abstract

A newly developed MMIC FET variable attenuator has demonstrated a 30dB dynamic range of attenuation over a DC-50GHz frequency band with a minimum insertion loss of 1.8dB at 26.5GHz and 2.6dB at 40GHz. The maximum attenuation increases with frequency from 32dB at DC to 42dB at 50GHz.

I. Introduction

A variety of MMIC variable attenuators have appeared in the literature and become available in the commercial market which utilizes GaAs MESFETs as voltage- controlled variable resistors [1][2][3]. The designs of these attenuators, with almost no exception, rely on a basic T- or π-configuration which is well represented by Tajima's work [1]. In this basic configuration, however, parasitic capacitances of FETs degrades the high-frequency performance of an attenuator both at a minimum insertion state and at a maximum attenuation state, limiting practical operation beyond 20GHz. This paper describes the design and the performance of a new MMIC FET variable attenuator which has achieved a DC-50GHz operation with a 30dB dynamic attenuation range by incorporating novel circuit techniques developed to circumvent the parasitic capacitance problem.

II. Design of Attenuator

Fig.1 shows an rf circuit schematic of the new attenuator. Although it basically employs a T-configuration, the new attenuator destributed a shunt FET into four cells interconnected by a length of high impedance transmission lines. At a minimum attenuation setting when shunt FETs are equivalently represented as capacitances, the distributed structure absorbs the FET capacitances into an artificial 50 ohm transmission line. At a maximum attenuation setting with the shunt FETs effectively functioning as low resistances, the distributed LR structure yields increased attenuation with frequency, thus compensating for degraded isolation due to parasitic capacitances of the series FETs. Furthermore, a 50 ohm resistor connected in parallel with each series FET minimizes the parasitic capacitances at the maximum attenuation setting by allowing the series FETs to be biased well below their pinch-off voltage. The resistors also eliminate the otherwise necessary adjustment of the V1 control voltage to bring a series FET resistance to 50 ohm. The use of the pure 50 ohm

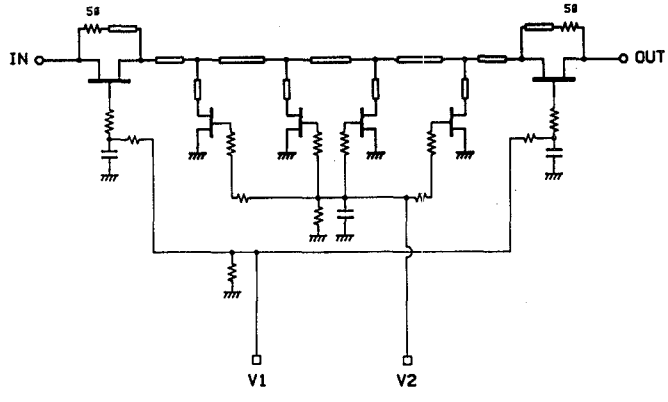

Fig.1. RF circuit schematic of the new DC-50GHz MMIC attenuator.

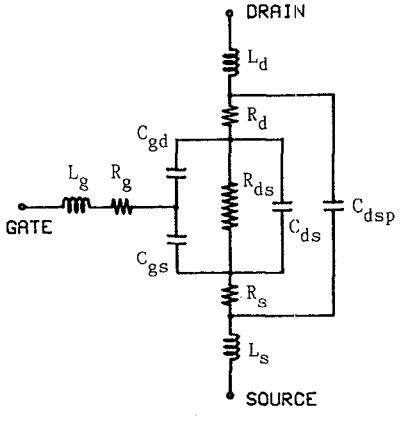

Fig.2. An equivalent circuit of an FET biased at Vds=0V.

0149-645X/88/0000-0499$01.00 © 1988 IEEE

resistors also reduces large-signal harmonic distortion levels at high attenuation settings due to their linearity inherently better than FETs.

A first-order analysis of the circuit shows that Eq. (1) must be satisfied for the entire attenuator to achieve increased attenuation with frequency at the maximum attenuation setting.

$$N \gtrsim 4\pi f_c \sqrt{\frac{2 \cdot 50 \cdot C_{50}}{(\frac{G_{ON}}{C_{ON}})(\frac{C_{ON}}{C_{OFF}})}} \qquad (1)$$

where N is the number of shunt FET cells, f_c being a cut-off frequency of the artificial 50 ohm transmission line at the minimum attenuation setting. G_{ON} and C_{ON} are the effective conductance and capacitance of a shunt FET cell in its ON state, respectively, and C_{OFF} is the effective capacitance of the cell biased below its pinch-off voltage. C_{50} is the effective capacitance of a series FET combined with a parallel resistor for the overall resistance value adjusted to 50 ohms.

The circuit design was optimized on SuperCompact using an FET equivalent circuit depicted in Fig.2. The FET model was derived from measured S-parameters using a similar technique described in reference [4]. Each element value was then expressed as a function of gate voltage to be used in the optimization process.

Fig.3 shows an entire chip layout of the new attenuator including a DC reference circuit the functions of which will be explained later. The chip measures 1.52 x 0.65 mm^2 (60 x 26 mil^2) with 100μm substrate thickness. The gate peripheries of 750μm and 200μm were chosen for a seires FET and a shunt FET, respectively. The circuit was fabricated on an MBE grown epitaxical layer with $3x10^{17} cm^{-3}$ doping concentration, using a 0.5μm-gate MMIC process summarized in reference [5]. A tantalum nitride thin film process was used to realize the 50 ohm resistors.

III. Measured Performance

Fig.4 shows the attenuator performance measured over a DC-50GHz frequency range using a Cascade Microtech on-wafer probe station. Each curve in the figure represents a different attenuation setting in a roughly 5dB step, for which a proper combination of the control voltages, V1 and V2, was chosed to simultaneously obtain good input/output impedance metching. The attenuator achieved a minimum insertion loss of 1.8dB, 2.6dB and 4.2dB at 26.5GHz, 40GHz and 50GHz, respectively, with a greater than 30dB dynamic attenuation range over the entire frequency band. The maximum attenuation increased with frequency from 32dB at DC to 42dB above 26GHz. The associated input/output return loss was always greater than 10dB at any attenuation setting for a 30dB dynamic range. When used

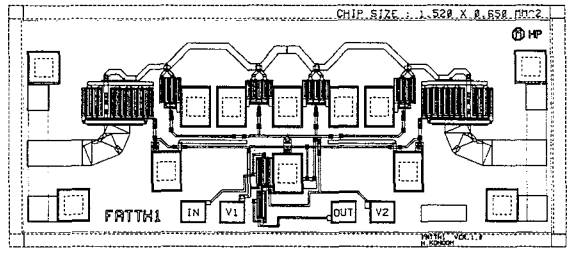

Fig.3. MMIC chip layout of the new attenuator. The chip measures 1.52x0.65 mm^2.

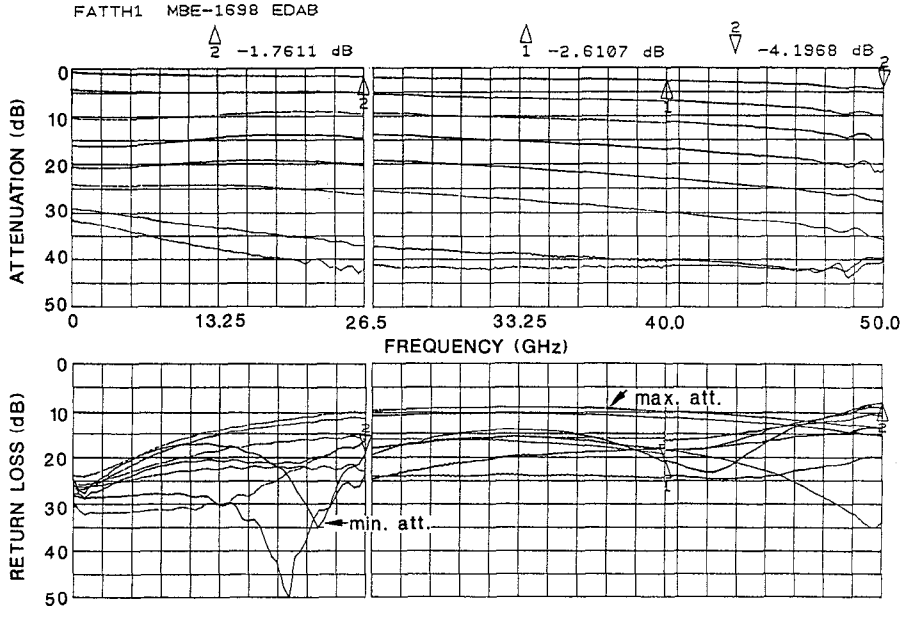

Fig. 4. Attenuator performance measured over a DC-50GHz frequency range.

as a SPST switch, the attenuator demonstrated a less than 1 nsec switching time.

Fig.5 shows a circuit schematic of an entire attenuator chip along with external operational amplifier feedback circuits connected to the on-chip DC reference circuit. The DC reference circuit replicates the rf attenuator circuit at a 10 times higher impedance level with a 500 ohm characteristic impedance and is controlled by the same control voltages that control the rf circuit. A dc reference voltage, V_{REF}, with a 500 ohm series resistor simulates an rf source. The left-hand operational amplifier monitors the input impedance of the DC reference circuit against a 500 ohm reference resistor and adjusts the V1 voltage to achieve good input/output impedance matching. The right-hand operational amplifier realizes linear attenuation vs. a single control voltage, V_{IN}, by monitoring the output signal from the DC reference circuit to adjust the V2 voltage. Fig.6 plots the attenuation characteristics measured as a function of the V_{IN} control voltage, where reasonable linearity can be seen for a signal frequency ranging from 300KHz to 26.5GHz. The implementation of the feedback scheme caused no noticeable change in rf attenuator performance.

The feedback scheme also reduces the temperature coefficient of attenuation since the DC reference circuit thermally tracks the rf attenuator circuit. Fig.7 shows the relative change of attenuation for an ambient temperature between 15°C and 45°C. The highest attenuation sensitivity, observed around a 10dB attenuation setting, was 0.2dB/100°C with the feedback loop, compared with 1.2dB/100°C without it.

IV. Conclusion

A newly developed MMIC variable attenuator has demonstrated a 30dB dynamic range of attenuation over a DC-50GHz frequency band with a minimum insertion loss of 1.8dB at 26.5GHz and 2.6dB at 40GHz. The associated input/output return loss was always greater than 10dB at any attenuation setting. An operational amplifier feedback scheme implemented around a DC reference circuit enabled automatic input/output impedance matching and linear attenuation with a single control voltage without any noticeable degradation of rf performance.

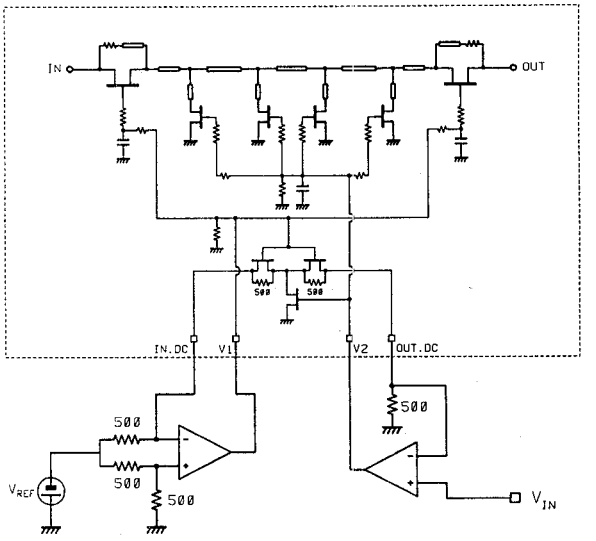

Fig.5. A circuit schematic of the entire attenuator chip with external operational amplifier feedback circuits connected to the on-chip DC reference circuit.

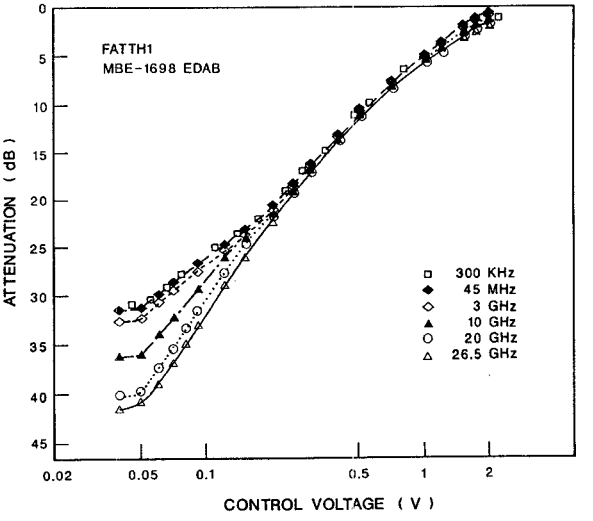

Fig.6. Attenuation linearity obtained by using the DC reference circuit feedback loop.

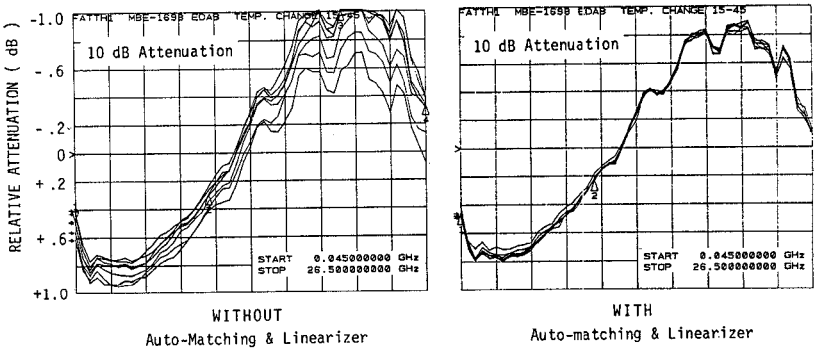

Fig.7. Attenuation sensitivity to the ambient temperature, measured with and without the DC reference circuit feedback loop. The highest sensitivity was observed around a 10dB attenuation setting.

Acknowledgement

The author would like to acknowledge Don Estreich, Jerry Gladstone and Derry Hornbuckle for their continuing encouragement and fruitful discussions. A patent is pending for the attenuator circuit.

References

[1] Y. Tajima et al., "GaAs Monolithic wide-band(2-18GHz) variable attenuators," IEEE MTT-S Digest, pp.479-481, 1982.

[2] G.S. Barta et al., "A 2 to 8 GHz leveling loop using a GaAs MMIC active splitter and attenuator," IEEE Microwave and mm-wave Monolithic Circuit Symposium Digest, pp.75-79, 1986.

[3] J.P. Mondal et al., "Theoretical analysis for microwave T- and π-type attenuator circuits using MESFETs," Int. J. Electronics, vol.58, no.2, pp.231-247, 1985.

[4] H. Kondoh, "An accurate FET modelling from measured S-parameters," IEEE MTT-S Digest, pp.377-380, 1986.

[5] D. D'Avanzo and T. Taylor, "An evaluation of deep UV lithography for 0.5 μm microwave GaAs IC's," Proc. Cornell Conference on High-Speed Semiconductor Devices & Circuits, pp,147-156, Aug. 1983.